A High Resolution, Low Offset Voltage, Gain Stability Comparator

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Abstract: Comparators are widely used in data converters. This paper proposes a voltage comparator circuit based on 180nm in cadence platform virtuoso tool BiCMOS process. In order to get stable gain in all temperatures, two kinds of temperature coefficient bias current are used, one for BJT differential pair, and another for CMOS differential pair. By using three-level amplifier and the special output stage the voltage gain is 40dB. The maximum voltage gain variation is 2dB when the temperature from -40°C to 100°C. Compared with conventional PWM existing comparators, the proposed system advantages are fast response, low offset voltage, high resolution and gain stability. The proposed comparator is applied to a buck converter.

Index Terms: Resolution, Stable Gain, Comparator

I. INTRODUCTION

Now a day in this digital world analog output signals are converts into digital form using ADCs. Comparator is the basic component used to interface to the digital logic [5]. The basic comparator consists of three blocks shown in below

Fig.1 Block diagram of comparator

In the recent years portable and battery-powered equipment getting smaller and smaller which means the switching converters should decrease the volume of outer devices by increase the switching frequency. There are a lot of comparators in the power management ICs. And, their performance limited the switching frequency of the converters. The environment of the power management ICs is changing over time, such as the load, the input voltage, the temperature. So comparator should have low offset voltage, low transmission delay, and a stable voltage gain in various temperatures, to make the systems remain stable [1]. It is a suitable voltage comparator for high resolution and gain stability application.

This paper organized as follows: Section II describe the operation of existing system. Section III describes the proposed system. Section IV simulation results and section V conclusion of the work done.

II EXISTING SYSTEM

Generally, the comparator for the data converter implemented in BiCMOS process. BJT’s are used to get high speed operation and MOSFET’s are used for low quiescent current. The comparator is basically composed of NPN amplifier, CMOS amplifier, emitter follower and sooch - cascode current mirror. Sooch current mirror is used to increase the output impedance [1]. In the same bias condition, bipolar transistors have larger transconductance and higher speed than MOS transistors [3]. But in data converters comparator design is one of the major concerns for meeting specifications such as resolution, conversion rate, input voltage range, power dissipation, and area[3],[4]. For small battery operated IC’s require low offset voltage and high resolution also.

Comparator consists of three blocks preamplifier, decision circuit and output buffer stage. In the existing system the first two stages BJT differential amplifiers with resistive load and last stage CMOS amplifier with active load. After preamplifier output is connected
through the buffers and buffers are CC amplifiers. And second stage output is connected some special transistors to drive the CMOS stage shown in the figure 2. Using MOSFET at the output stage the gain will increase.

Using CMOS inverter gate at the output stage the rise time and fall time of the output will be decreased. PTC bias current at NPN side and NTC bias current at the CMOS side are used to get stable gain and delay at various temperatures.

IV SIMULATION RESULTS

The simulation is done by using cadence gpdk-180nm Technology spectra simulator. The results of proposed design are shown in figures 3-6. Figure 3 shows the DC response of the proposed design. Figure 4 is the gain of the proposed comparator and maximum gain variation from -40°C to 100°C is 2dB. Figure 5 shows the off-set voltage at 25°C. Resolution of the proposed comparator is 1.1mv up to 100 Mhz shown in figure 6.

III PROPOSED SYSTEM

The proposed architecture have track and latch circuit at the second stage i.e. decision stage. By using this circuit the resolution of the comparator will be improved. And using output stage with CMOS amplifier output swing will be reduced.

In the track and latch circuit the W/L ratio of the PMOS transistors will be increased [5] for increase current. The following diagram is the proposed system design.
V CONCLUSION

It is a suitable voltage comparator for high resolution and gain stability application. By using the track and latch circuit and output CMOS stage to achieve the 40db voltage gain, 15uv offset voltage, 1mv resolution and by using two kinds of bias current to have a stable gain and delay.

REFERENCES

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